

牛芯半导体（深圳）有限公司

**KNIULINK Co., Ltd.**

NS69993 Design Notes for rpcs.cmn Digital Block

Version 1.3

April 12, 2022

Revision History

|  |  |  |  |
| --- | --- | --- | --- |
| Ver. # | Rev. Date | Rev. By | Comment |
| 1.0 | 2022/2/25 | CaoHuiyang | Initial version |
| 1.1 | 2022/3/05 | CaoHuiyang | Add inter-structure and function |
| 1.2 | 2022/3/10 | CaoHuiyang | Supplement to reg\_arbt |
| 1.3 | 2022/4/12 | CaoHuiyang | update |

**Contents**

[NS69993 Design Notes for rpcs.cmn Digital Block 0](#_Toc28149)

[1 Spec/Function Requirement/Function Description 3](#_Toc18709)

[2 Signal Definition 4](#_Toc12491)

[3 Implementation Details 12](#_Toc24857)

[3.1 Clock & Reset 12](#_Toc25035)

[3.2 Hardware Implementation 12](#_Toc4881)

[3.2.1 cmn\_creg 12](#_Toc27804)

[3.2.2 creg\_ctl 15](#_Toc16783)

[3.2.3 reg\_arbt 17](#_Toc24810)

[3.2.4 mem 20](#_Toc8045)

[3.2.5 mem\_arbt 22](#_Toc26777)

[3.2.6 mem\_reg0 23](#_Toc12201)

[3.2.7 mem\_reg1 25](#_Toc8369)

[3.2.8 mem\_reg2 25](#_Toc12576)

[3.2.9 mem\_reg3 25](#_Toc29355)

[3.2.10 reg\_mapping 26](#_Toc15672)

[3.3 Hardware summarize 27](#_Toc14583)

[4 User guide 28](#_Toc22709)

[4.1 Configuration Requirements 28](#_Toc4350)

[4.3 Registers 28](#_Toc28743)

[5 Special Note 28](#_Toc3566)

[6 FPGA Verification 28](#_Toc18080)

[7 Test Mode Strategy 28](#_Toc23303)

[8 Simulation List 28](#_Toc18442)

# Spec/Function Requirement/Function Description

* Register Management and Mapping
* Lanes.fsm’s Memory and Memory Management
* Jtag/cr\_apb\_interface mux to cr\_interface

# Signal Definition

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Signal name** | | **I/O** | **From** | **To** | **Description/Function** |
| cr\_ext\_clk | | input | aon |  | cr external clock |
| cr\_ext\_clk\_rst | | input |  | cr external clock reset· |
| cr\_clk | | input |  | cr clock |
| cr\_rst | | input |  | cr reset |
| phy\_func\_reset | | output |  | aon |  |
|  | |  |  |  |  |
| ref\_range | | input | pcs\_raw |  |  |
| rx\_term\_offset[4:0] | | input | pcs\_raw |  | rx terminating resistor offset |
| txup\_term\_offset[8:0] | | input |  | rx pull-up resistor offset |
| txdn term\_offset[8:0] | | input |  | rx pull-down resistor offset |
| rtune\_req | | input |  | rtune require |
| fw\_pwrup done\_r | | output |  | aon | Send fw\_pwrup\_done\_r to AON cmn for MPLL force/skip logic |
|  | |  |  |  |  |
| fw\_rdy | | output |  | pcs\_raw\_lane | Generate fw\_rdy signal to lanes  always high |
| pma\_rx\_term\_offset  [4:0] | | output |  | pcs\_raw->PMA | rx terminating resistor to pma |
| pma\_txup\_term\_offset[8:0] | | output |  | rx pull-up resistor offset to pma |
| pma\_txdn\_term\_offset[8:0] | | output |  | rx pull-down resistor offset to pma |
|  | |  |  |  |  |
| pma\_rtune\_req | | output |  | pcs\_raw->PMA | Rtune require to pma |
|  | |  |  |  |  |
| cr\_para seli | | input | aon |  | from aon block--jtag and apb\_cr mux control signal(bus switch signal) |
| cr\_para\_addr[16:0] | | input | pcs\_raw |  | CREG parallel interface（cr bus）  (from apb or jtag) |
| cr\_para\_wr\_en | | input |  |
| cr\_para\_wr\_data[16:0] | | input |  |
| cr\_para\_rd\_en | | input |  |
| cr\_para\_rd\_data[16:0] | | output |  | pcs\_raw |
| cr\_para\_ack | | output |  |
| **Signal name** | | **I/O** | **From** | **To** | **Description/Function** |
| cr\_cmn\_aon sel[31:0] | output | |  | pcsraw\_aon\_cmn | aon register select control（decoding generated select to the registers in aon module） |
| cr\_cmn\_aon\_sel2[31:0] | output | |  |
| cr\_cmn\_aon\_rd\_data[15:0] | input | | pcsraw\_aon\_cmn |  | aon register read back data（read back data from the registers in aon module） |
| Jtag\_trst\_n | input | | pcs\_raw |  | Jtag reset |
| jtag\_clk | input | | pcsraw\_aon\_cmn |  | Jtag clock |
| jtag\_clk\_n | input | |  | Jtag clock |
| jtag\_tms | input | | pcs\_raw |  | Jtag bus |
| jtag tdi | input | |  |
| jtag tdo | output | |  | pcs\_raw |
| jtag tdo\_en | output | |  |
| jtag\_apb\_sel | output | |  |  | If jtag\_apb\_sel=1,then apb be active |
| ovrd\_clk\_sel | output | |  | aon |  |
| ovrd\_rst\_sel | output | |  |  |
| phy\_reset\_ov | output | |  |  |
| txrx0\_reset\_ov | output | |  |  |
| txrx1\_reset\_ov | output | |  |  |
| txrx2\_reset\_ov | output | |  |  |
| txrx3\_reset\_ov | output | |  |  |
| scan\_mode | input | | From pcs\_raw and input aon at the same time |  |  |
| scan\_shift | input | |  |  |
| scan shift\_cg | input | |  |  |
| scan\_set\_rst | input | |  |  |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| cr\_addr[15:0] | output |  | Raw PCS lane and PMA registers | CREG parallel interface (for Raw PCS lane and PMA registers)  (to Raw PCS lane and PMA) |
| cr\_wr\_en | output |  |
| cr\_wr\_data[15:0] | output |  |
| cr\_rd\_en | output |  |
|  |  |  |  |  |
| cr\_pma\_rd\_data[15:0] | input | PMA->pcs\_raw |  | CREG read data from PMA |
| **Signal name** | **I/O** | **From** | **To** | **Description/Function** |
| cr0\_rd\_data[15:0] | input | Raw PCS lanes |  | CREG read data from Raw PCS lanes(lane0-3,lane4-7 no use) |
| cr1\_rd\_data[15:0] | input |  |
| cr2\_rd\_data[15:0] | input |  |
| cr3\_rd\_data[15:0] | input |  |
| cr4\_rd\_data[15:0] | input |  |
| cr5\_rd\_data[15:0] | input |  |
| cr6\_rd\_data[15:0] | input |  |
| cr7\_rd\_data[15:0] | input |  |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| cr0\_mem\_ack | output |  | Raw PCS  lanes | CREG interface with Memory-Arbiter((memory bus be used by lane.fsm,  lane0-3,lane4-7 no use)) |
| cr1\_mem\_ack | output |  |
| cr2\_mem\_ack | output |  |
| cr3\_mem\_ack | output |  |
| cr4\_mem\_ack | output |  |
| cr5\_mem\_ack | output |  |
| cr6\_mem\_ack | output |  |
| cr7\_mem\_ack | output |  |
|  |  |  |  |
| cr0\_mem\_rd\_data  [15:0] | output |  | Raw PCS lanes |
| cr1\_mem\_rd\_data  [15:0] | output |  |
| cr2\_mem\_rd\_data  [15:0] | output |  |
| cr3\_mem\_rd\_data  [15:0] | output |  |
| Cr4\_mem\_rd\_data  [15:0] | output |  |
| cr5\_mem\_rd\_data  [15:0] | output |  |
| cr6\_mem\_rd\_data  [15:0] | output |  |
| cr7\_mem\_rd\_data  [15:0] | output |  |
|  |  |  |  |
| cr0\_mem\_req | input | Raw PCS lanes |  |
| cr1\_mem\_req | input |  |
| cr2\_mem\_req | input |  |
| cr3\_mem\_req | input |  |
| cr4\_mem\_req | input |  |
| cr5\_mem\_req | input |  |
| cr6\_mem\_req | input |  |
| cr7\_mem\_req | input |  |
|  |  |  |  |
| cr0\_mem\_addr[15:0] | input | Raw PCS lanes |  |
| cr1\_mem\_addr[15:0] | input |  |
| cr2\_mem\_addr[15:0] | input |  |
| cr3\_mem\_addr[15:0] | input |  |
| cr4\_mem\_addr[15:0] | input |  |
| cr5\_mem\_addr[15:0] | input |  |
| cr6\_mem\_addr[15:0] | input |  |
| cr7\_mem\_addr[15:0] | input |  |
|  |  |  |  |
| cr0\_mem\_wr\_en | input | Raw PCS lanes |  |
| cr1\_mem\_wr\_en | input |  |
| cr2\_mem\_wr\_en | input |  |
| cr3\_mem\_wr\_en | input |  |
| cr4\_mem\_wr\_en | input |  |
| cr5\_mem\_wr\_en | input |  |
| cr6\_mem\_wr\_en | input |  |
| cr7\_mem\_wr\_en | input |  |
|  |  |  |  |
| cr0\_mem\_wr\_data  [15:0] | input | Raw PCS lanes |  |
| cr1\_mem\_wr\_data  [15:0] | input |  |
| cr2\_mem\_wr\_data  [15:0] | input |  |
| cr3\_mem\_wr\_data  [15:0] | input |  |
| cr4\_mem\_wr\_data  [15:0] | input |  |
| cr5\_mem\_wr\_data  [15:0] | input |  |
| cr6\_mem\_wr\_data  [15:0] | input |  |
| cr7\_mem\_wr\_data  [15:0] | input |  |
|  |  |  |  |
| cr0\_mem\_rd\_en | input | Raw PCS lanes |  |
| cr1\_mem\_rd\_en | input |  |
| cr2\_mem\_rd\_en | input |  |
| cr3\_mem\_rd\_en | input |  |
| cr4\_mem\_rd\_en | input |  |
| cr5\_mem\_rd\_en | input |  |
| cr6\_mem\_rd\_en | input |  |
| cr7\_mem\_rd\_en | input |  |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| cr0\_reg\_ack | output |  | Raw PCS lanes | CREG interface with Register-Arbiter  (The address generated by decoding is register map address exactly.) |
| cr1\_reg\_ack | output |  |
| cr2\_reg ack | output |  |
| cr3\_reg\_ack | output |  |
| cr4\_reg\_ack | output |  |
| cr5\_reg\_ack | output |  |
| cr6\_reg\_ack | output |  |
| cr7\_reg\_ack | output |  |
|  |  |  |  |
| cr0\_reg\_rd\_data[15:0] | output |  | Raw PCS lanes |
| cr1\_reg\_rd\_data[15:0] | output |  |
| cr2\_reg\_rd\_data[15:0] | output |  |
| cr3\_reg\_rd\_data[15:0] | output |  |
| cr4\_reg\_rd\_data[15:0] | output |  |
| cr5\_reg\_rd\_data[15:0] | output |  |
| cr6\_reg\_rd\_data[15:0] | output |  |
| cr7\_reg\_rd\_data[15:0] | output |  |
|  |  |  |  |
| cr0\_reg\_req | input | Raw PCS lanes |  |
| cr1\_reg\_req | input |  |
| cr2\_reg\_req | input |  |
| cr3\_reg\_req | input |  |
| cr4\_reg\_req | input |  |
| cr5\_reg\_req | input |  |
| cr6\_reg\_req | input |  |
| cr7\_reg\_req | input |  |
|  |  |  |  |
| cr0\_reg\_addr[15:0] | input | Raw PCS lanes |  |
| cr1\_reg\_addr[15:0] | input |  |
| cr2\_reg\_addr[15:0] | input |  |
| cr3\_reg addr[15:0] | input |  |
| cr4\_reg\_addr[15:0] | input |  |
| cr5\_reg\_addr[15:0] | input |  |
| cr6\_reg\_addr[15:0] | input |  |
| cr7\_reg\_addr[15:0] | input |  |
|  |  |  |  |
| cr0\_reg\_wr\_en | input | Raw PCS lanes |  |
| cr1\_reg\_wr\_en | input |  |
| cr2\_reg\_wr\_en | input |  |
| cr3\_reg\_wr\_en | input |  |
| cr4\_reg\_wr\_en | input |  |
| cr5\_reg\_wr\_en | input |  |
| cr6\_reg\_wr\_en | input |  |
| cr7\_reg\_wr\_en | input |  |
|  |  |  |  |
| cr0\_reg\_wr\_data[15:0] | input | Raw PCS lanes |  |
| cr1\_reg\_wr\_data[15:0] | input |  |
| cr2 reg\_wr\_data[15:0] | input |  |
| cr3\_reg\_wr\_data[15:0] | input |  |
| cr4\_reg\_wr\_data[15:0] | input |  |
| cr5\_reg\_wr\_data[15:0] | input |  |
| cr6\_reg\_wr\_data[15:0] | input |  |
| cr7\_reg\_wr\_data[15:0] | input |  |

# Implementation Details

## Clock & Reset

**cr\_ext\_clk** be generated from **aon\_cmn**,switch from **cr\_jtag\_clk** or **cr\_para\_clk** by **cr\_para\_sel\_i** selected.

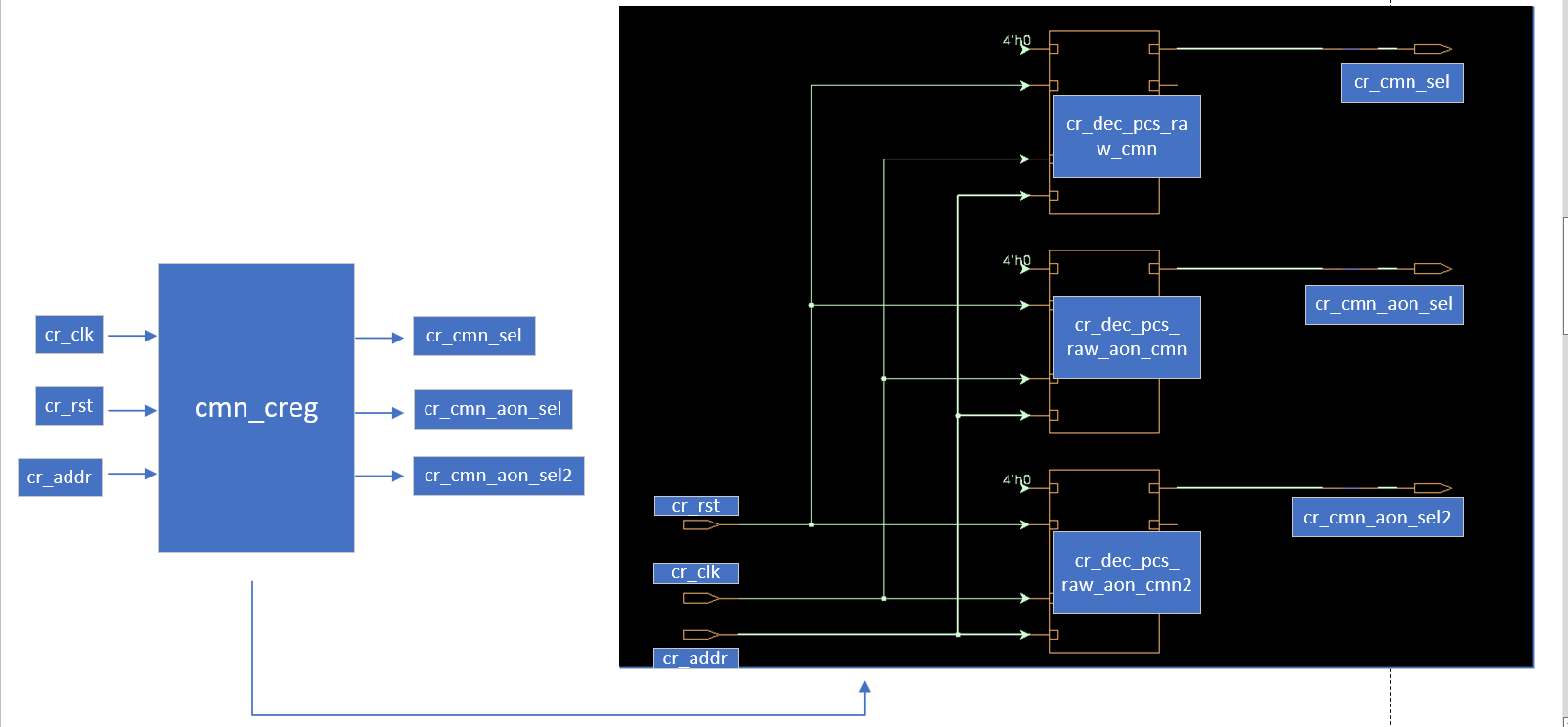
**cr\_ext\_clk\_rst** be come from **phy\_reset\_i** is synchronized by **cr\_ext\_clk**.

**cr\_rst** is synchronized by **cr\_clk**,come from **aon\_cmn**,be generated by **phy\_reset\_i** and **scan\_set\_rst**.

## Hardware Implementation

### cmn\_creg

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Signal name** | **I/O** | **From** | **To** | **Description/Function** |
| cr\_cmn\_sel[31:0] | output |  | pcs\_raw\_cmn | pcs\_raw\_cmn interal regsiter select |
| cr\_cmn\_aon\_sel[31:0] | output |  | pcs\_raw\_aon\_cmn | pcs\_raw\_aon\_cmn regsiter select |
| cr\_cmn\_aon\_sel2[31:0] | output |  | pcs\_raw\_aon\_cmn | pcs\_raw\_aon\_cmn regsiter select |
|  |  |  |  |  |
| cr\_clk | input | pcs\_raw\_cmn |  | cr clock |
| cr\_rst | input | pcs\_raw\_cmn |  | cr reset |
| cr\_addr[15:0] | input | pcs\_raw\_cmn |  | cr address bus(is register map address exactly) |



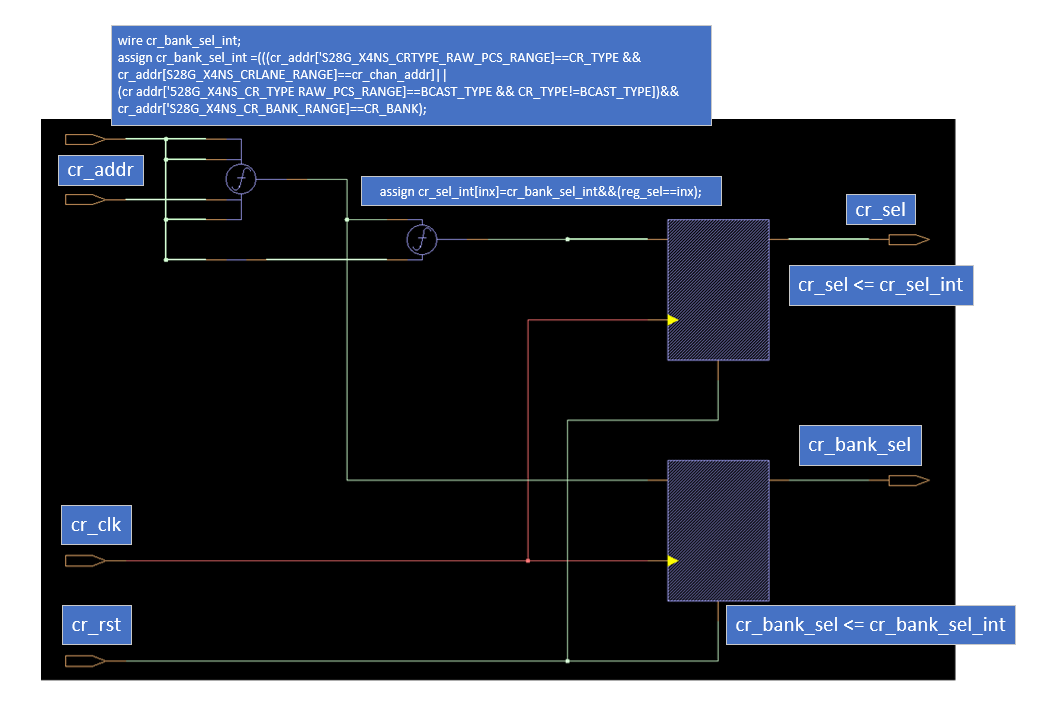
As shown in FIG, **cmn\_creg** module include **cr\_dec\_pcs\_raw\_cmn** module/**cr\_dec\_pcs\_raw\_aon\_cmn** module and **cr\_dec\_pcs\_raw\_aon\_cmn2** module.

The function of the **cmn\_creg** module is to use **cr\_addr** to generate the **pcs\_raw\_cmn** module’s internal registers chip select and the **pcs\_raw\_aon\_cmn** module’s registers chip select.

The function of the **cr\_dec\_pcs\_raw\_cmn** module is to use **cr\_addr** to decoding and generate the **cr\_cmn\_sel[31:0]** that is signal of chip select.

The function of the **cr\_dec\_pcs\_raw\_aon\_cmn** module is to use **cr\_addr** to decoding and generate the **cr\_cmn\_aon\_sel[31:0]** that is signal of chip select.

The function of the **cr\_dec\_pcs\_raw\_aon\_cmn2** module is to use **cr\_addr** to decoding and generate the **cr\_cmn\_aon\_sel2[31:0]** that is signal of chip select.

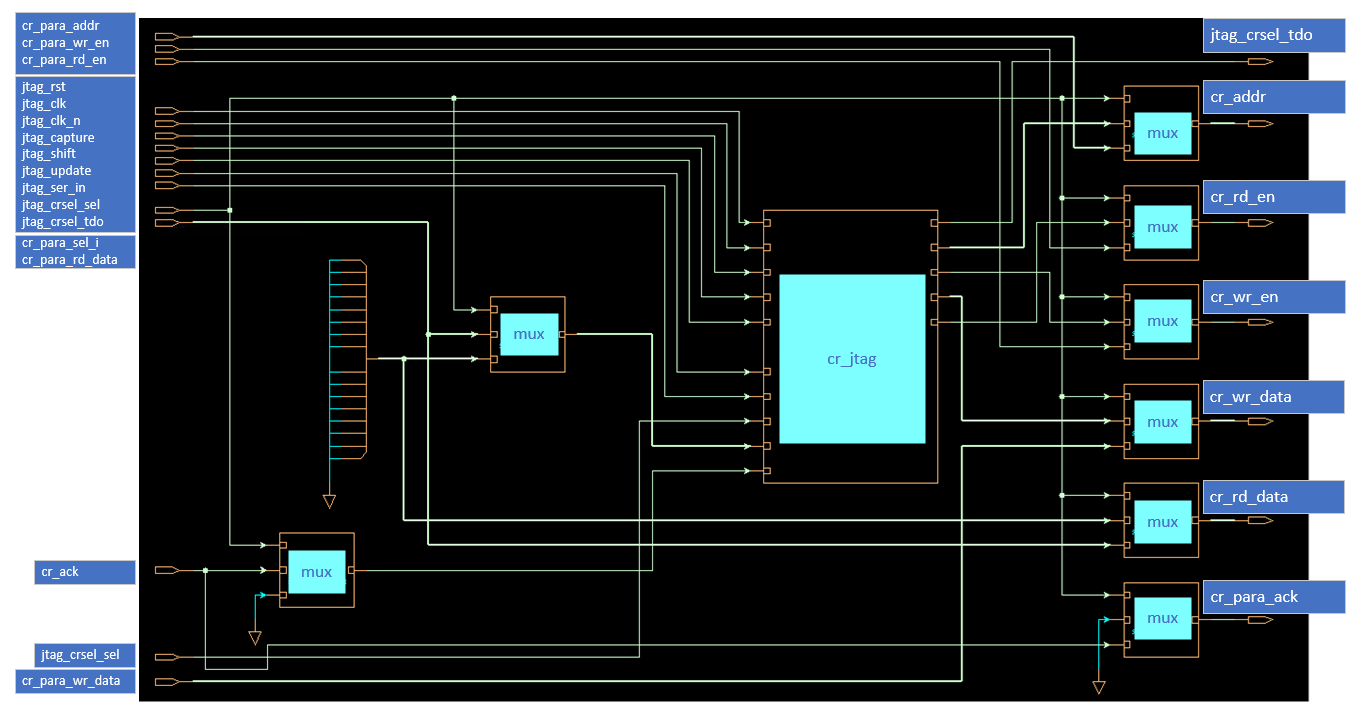


The interal structure of **cr\_dec\_pcs\_raw\_cmn/cr\_dec\_pcs\_raw\_aon\_cmn/cr\_dec\_pcs\_raw\_aon\_cmn2** modules are the same as shown in FIG,

After latching,the **cr\_addr** generated **cr\_sel** and **cr\_bank\_sel** by the decoding function **f1** and **f2**. In which **cr\_bank\_sel\_int** is the register bank chip select signal,**reg\_sel = cr\_addr[4:0]** is the number of registers in every modules. The **cr\_sel\_int** is the one-hot code represent of **reg\_sel**. The **cr\_bank\_sel** not be used, **cr\_sel** connected to the every correspond modules through three different buses,when **cmn\_creg** module instanted into **cr\_dec\_pcs\_raw\_cmn/cr\_dec\_pcs\_raw\_aon\_cmn/cr\_dec\_pcs\_raw\_aon\_cmn2** modules.

### creg\_ctl

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Signal name** | **I/O** | **From** | **To** | **Description/Function** |
| cr\_para\_sel\_i | input | cmn |  | APB OR JTAG SELECT |
|  |  |  |  |  |
| cr\_para\_addr[15:0] | input | cmn |  | CR Parallel Interface |
| cr\_para\_wr\_en | input |  |
| cr\_para\_wr\_data[15:0] | input |  |
| cr\_para\_rd\_en | input |  |
| cr\_para\_rd\_data[15:0] | output |  | cmn |
| cr\_para\_ac | output |  |
|  |  |  |  |  |
| jtag\_rst | input | jtag\_ctl |  | JTAG Register interface |
| jtag\_clk | input |  |
| jtag\_clk\_n | input |  |
| jtag\_capture | input |  |
| jtag\_shift | input |  |
| jtag\_update | input |  |
| jtag\_ser\_in | input |  |
| jtag\_crsel\_sel | input |  |
| jtag\_crsel\_tdo | output |  | jtag\_ctl |
|  |  |  |  |  |
| cr\_addr[15:0] | output |  |  | Internal CREG interface |
| cr\_wr\_en | output |  |
| cr\_wr\_data[15:0] | output |  |
| cr\_rd\_en | output |  |
| cr\_rd\_data[15:0] | input |  |  |
| cr\_ack | input |  |  |



The **creg\_ctl** module include **creg\_jtag** module,**cr\_addr\_mux** module,**cr\_wr\_data\_mux** module,**cr\_wr\_en\_mux** module,**cr\_rd\_en\_mux** module,**cr\_para\_rd\_data\_mux** module,**cr\_para\_ack\_mux** module,**cr\_jtag\_rd\_data\_mux** module and **cr\_jtag\_ack\_mux** module.

The function of the **cmn\_creg** module is switching **CR Parallel Interface**(default interface) and **JTAG Register interfac** to generate **Internal CREG interface** which process controled by **cr\_para\_sel\_i** signal.

The function of the **creg\_jtag** module is changing **JTAG Register interface** into **cr interfac**.

The function of the **cr\_addr\_mu** module is switching **cr\_jtag\_addr** and **cr\_para\_addr** to generate **cr\_addr** which process controled by **cr\_para\_sel\_i** signal.

The function of the **cr\_wr\_data\_mux** module is switching **cr\_jtag\_wr\_data** and **cr\_para\_wr\_data** to generate **cr\_wr\_data** which process controled by **cr\_para\_sel\_i** signal.

The function of the **cr\_wr\_en\_mux** module is switching **cr\_jtag\_wr\_en** and **cr\_para\_wr\_en** to generate **cr\_wr\_en** which process controled by **cr\_para\_sel\_i** signal.

The function of the **cr\_rd\_en\_mux** module is switching **cr\_jtag\_rd\_en** and **cr\_para\_rd\_en** to generate **cr\_rd\_en** which process controled by **cr\_para\_sel\_i** signal.

The function of the **cr\_para\_rd\_data\_mux** module is switching **0** and **cr\_rd\_data** to generate **cr\_para\_rd\_data** which process controled by **cr\_para\_sel\_i** signal.

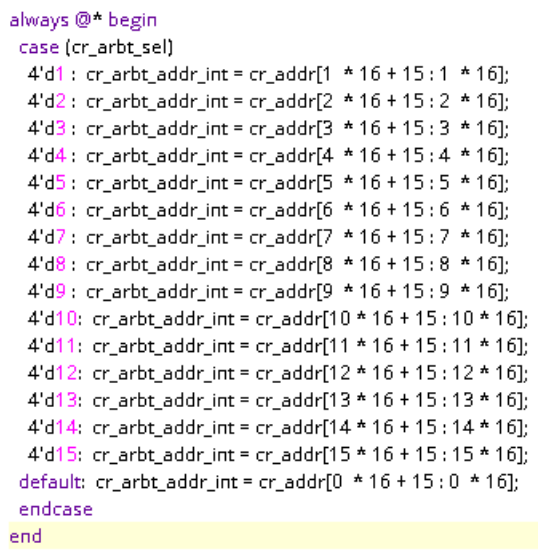
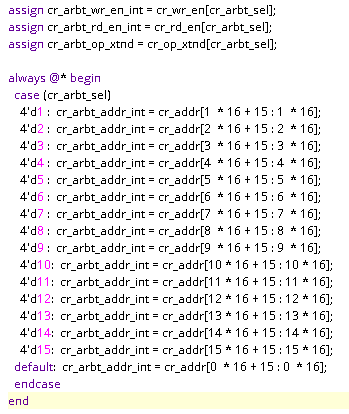
The function of the **cr\_para\_ack\_mux** module is switching **0** and **cr\_ack** to generate **cr\_para\_ack** which process controled by **cr\_para\_sel\_i** signal.

The function of the **cr\_jtag\_rd\_data\_mux** module is switching **0** and **cr\_rd\_data** to generate **cr\_jtag\_rd\_data** which process controled by **cr\_para\_sel\_i** signal.

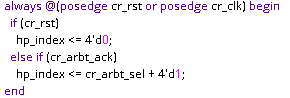
The function of the **cr\_jtag\_ack\_mux** module is switching **0** and **cr\_ack** to generate **cr\_jtag\_ack** which process controled by **cr\_para\_sel\_i** signal.

### reg\_arbt

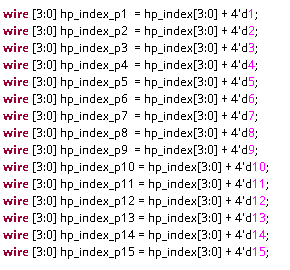
|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Signal name** | **I/O** | **From** | **To** | **Description/Function** |
| cr\_clk | input |  |  | Clock and Reset |
| cr\_rst | input |  |  |
|  |  |  |  |  |
| cr\_req[15:0] | input |  |  | CR input interfaces  (Combine the 16 cr interfaces into a 256-bit bus input, the address is the reg map address) |
| cr\_addr[255:0] | input |  |  |
| cr\_wr\_data[255:0] | input |  |  |
| cr\_wr\_en[15:0] | input |  |  |
| cr\_rd\_en[15:0] | input |  |  |
| cr\_op\_xtnd[15:0] | input |  |  |
| cr\_ack[15:0] | output |  |  |
| cr\_rd data[15:0] | output |  |  |
|  |  |  |  |  |
| cr\_arbt\_addr[15:0] | output |  |  | CR output interface(cr\_interface output after switch,the address is the reg map address） |
| cr\_arbt\_wr\_data[15:0] | output |  |  |
| cr\_arbt\_wr\_en | output |  |  |
| cr\_arbtrd\_en | output |  |  |
| cr\_arbt rd\_data[15:0] | input |  |  |



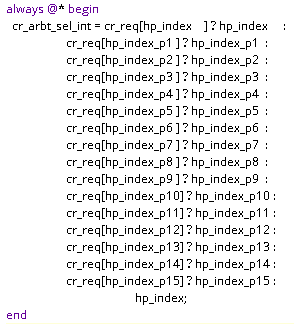
As shown above, **cr\_arbt\_sel (cr\_arbt\_sel\_int)** determines which **cr interface** is selected.



As shown above,if the current interface is selected,the value of **hp\_index** is the current selection value plus 1(**cr\_arbt\_sel**+1).



The above code indicates that **hp\_index\_p1...hp\_index\_p15** is the value of **hp\_index** plus 1..15, that is, the 16 interfaces is cyclically shifted left arrange from low to high based on the current be selected interface value.



Above code is the **cr\_arbt\_sel\_int** value generated process. Based on **hp\_index**, search for the position of **cr\_req[x]** where 1 first appears from low to high in the 16 interfaces(hp\_index->hp\_index\_p1->hp\_index\_p2...->hp\_index\_p14->hp\_index\_p15) ,the search process follows a round-robin selection pattern. If 1 is found, that interface is selected(**cr\_arbt\_sel\_int=hp\_index\_px**), if **cr\_req=0** (no request occurs) , **cr\_arbt\_sel\_int=hp\_index** (the current selected interface number value plus 1).

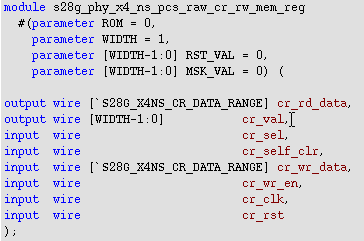
In summary, the function of the **reg\_arbt** module is to determine which of the 16 **CR input interfaces** is used as the **CR output interface** according to the value of **cr\_arbt\_sel**, and **cr\_arbt\_sel** is generated by **cr\_req** decoding. Specific process is the process of looping to the left to search the first be requested interface based on the currently selected interface.If cr\_req=0 (no request occurs), then cr\_arbt\_sel\_int=hp\_index (that is, the current selection path value plus 1).

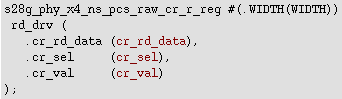
In this design, 4 interfaces are used, so the **reg\_arbt** module realizes the process of converting 4 **cr input interface** parallel input to 1 **CR output interface** serial output.

### mem

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Signal name** | **I/O** | **From** | **To** | **Description/Function** |
| cr\_c1k | input |  |  | Mem clock |
| cr\_rst | input |  |  | Mem reset |
|  |  |  |  |  |
| cr\_cmn[63:0]\_b[7:0]\_sel[31:0] | input | mem\_creg[3:0] |  | register select in mem |
|  |  |  |  |  |
| cr\_wr\_en | input |  |  | register write enable in mem |
| cr\_wr\_data[15:0] | input |  |  | register write data in mem |
| cr\_rd\_en | input |  |  | register read enable in mem |
| cr\_rd data[15:0] | output |  | Raw PCS lanes | register read data in mem |

The **mem** make up **cmn[63:0]\_b[7:0], b[7:0]** represent 8 mem banks, and **cmn[63:0]** represent 64 mem blocks, each mem block include 32 16bit registers, So if use 4 mem blocks, the memory size is 64（block）\*32（register）\*4（bank）=8192 registers (16bit). The memory unit is the register and the specific operation is as follows.





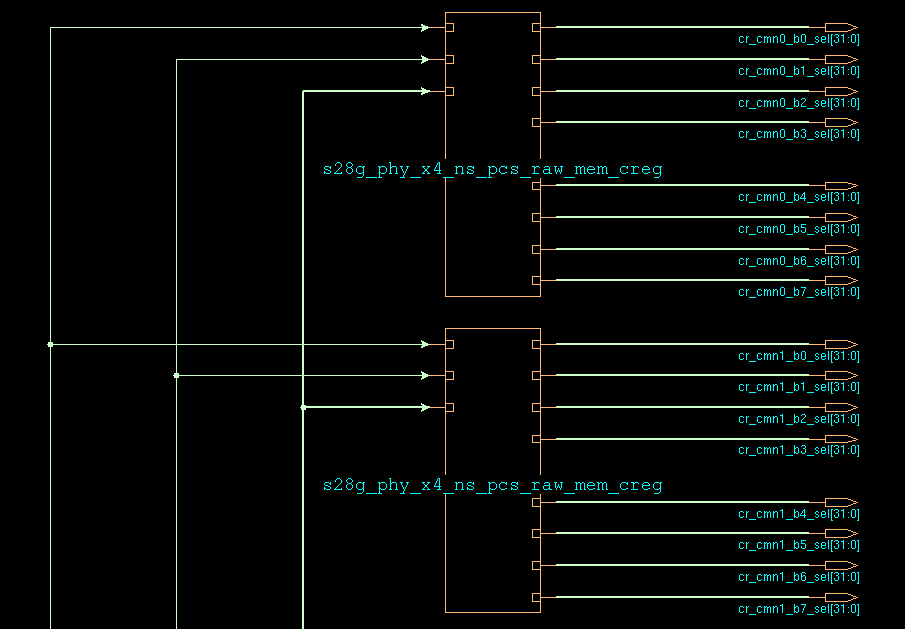
### mem\_arbt

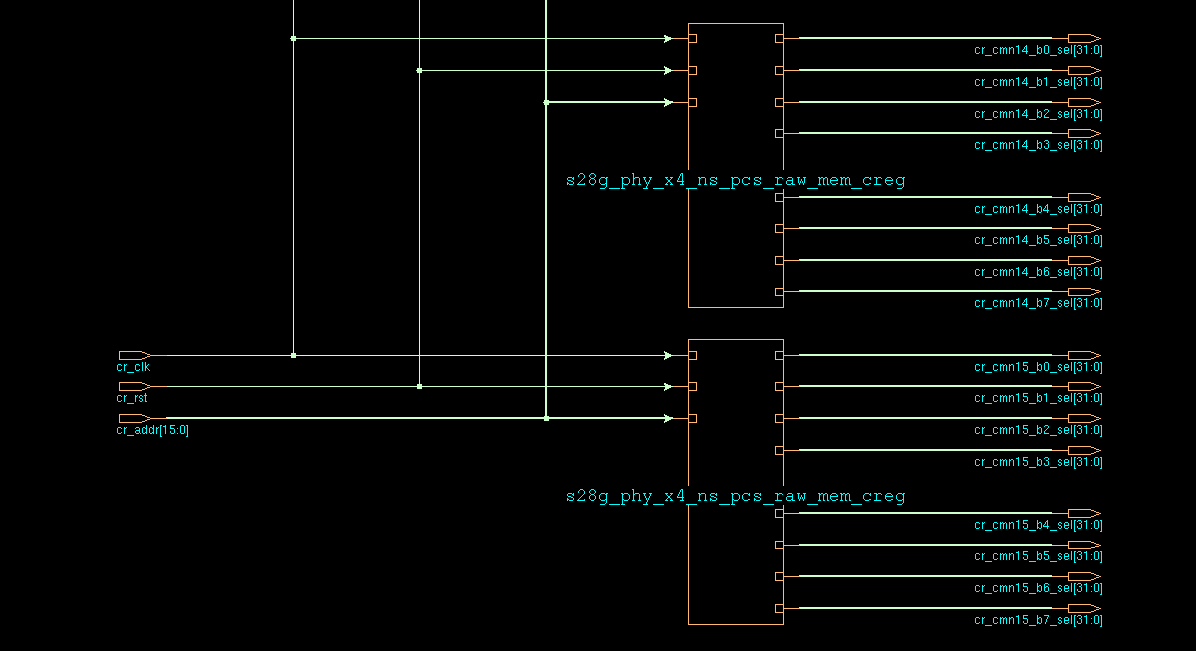
The interface and function of the **mem\_arb** module is the same as **reg\_arbt** module.The differnent is the input and output interface of **mem\_arb** module is data and address of **mem**.

### mem\_reg0

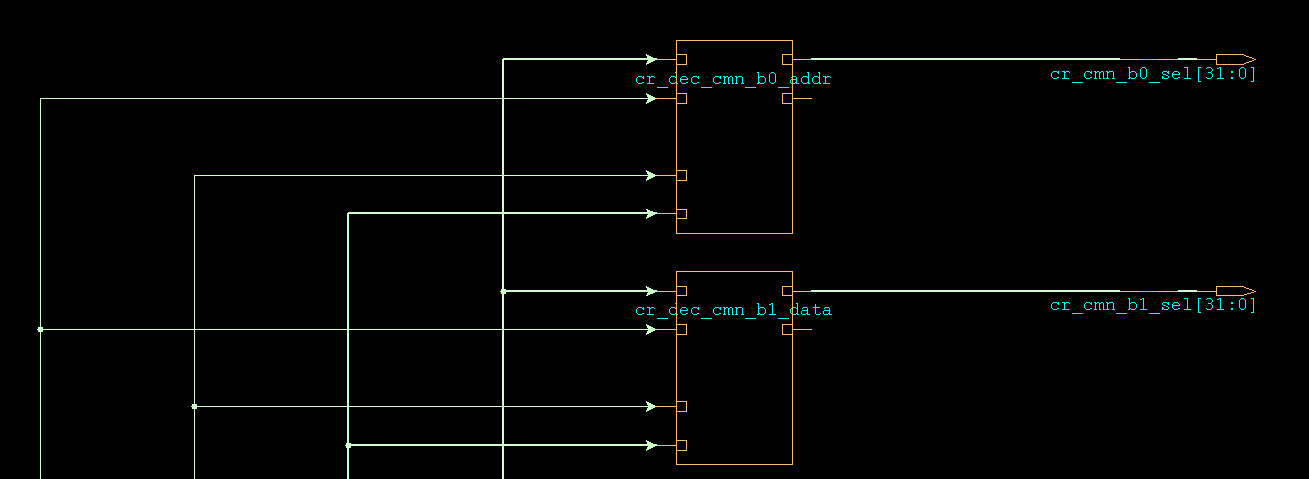
|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Signal name** | **I/O** | **From** | **To** | **Description/Function** |
| cr\_ck | input |  |  | mem clock |
| cr\_rst | input |  |  | mem reset |
| cr\_addr | input | Raw PCS lanes |  | mem address |
|  |  |  |  |  |
| cr\_cmn[15:0]\_b[7:0]\_sel | output |  | mem | register select in mem |

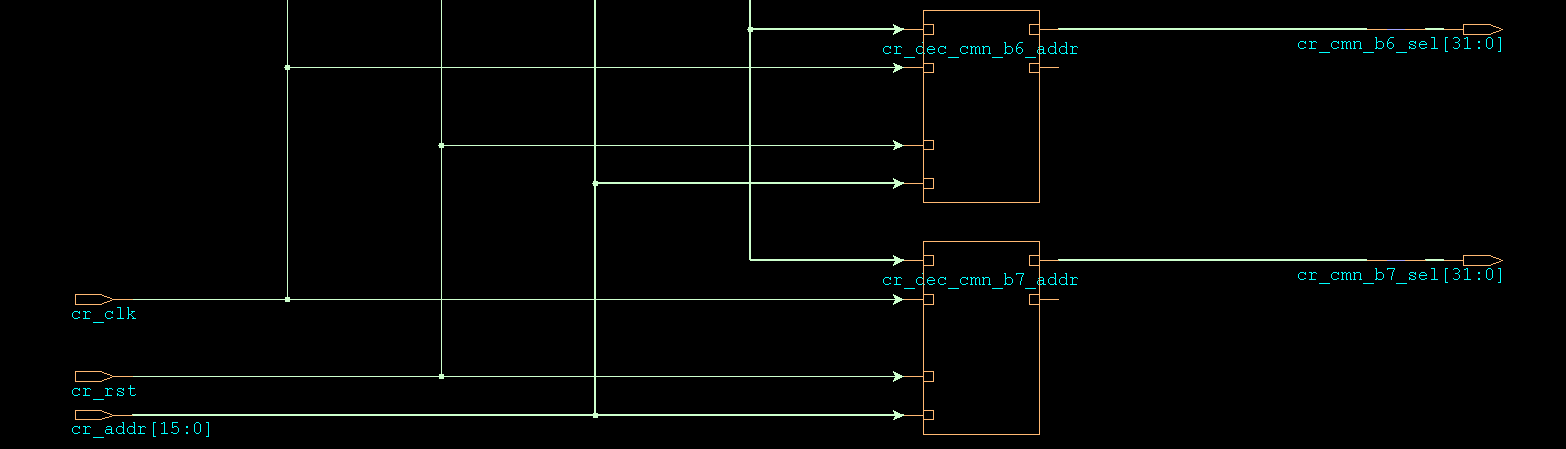
The function of the **mem\_reg** module is to generate the chip select signal of **cmn[15:0]\_b[7:0][31:0]** by decoding **cr\_addr[15:0]** (**cr\_addr** external connection **cr\_mem\_addr**).





The picture above is cmn0\_creg~cmn15\_creg (block select signal generate), and the lower picture is the internal structure of cmnX\_creg (bank select signal generate).





The internal structure of c**r\_dec\_cmn\_bx\_addr** module is the same as **cr\_dec\_pcs\_raw\_cmn/cr\_dec\_pcs\_raw\_aon\_cmn/cr\_dec\_pcs\_raw\_aon\_cmn2** modules.

### mem\_reg1

The interface and internal structure are the same as above.

Generate **cmn[31:16]\_b[7:0]** chip select.

### mem\_reg2

The interface and internal structure are the same as above.

Generate **cmn[47:32]\_b[7:0]** chip select.

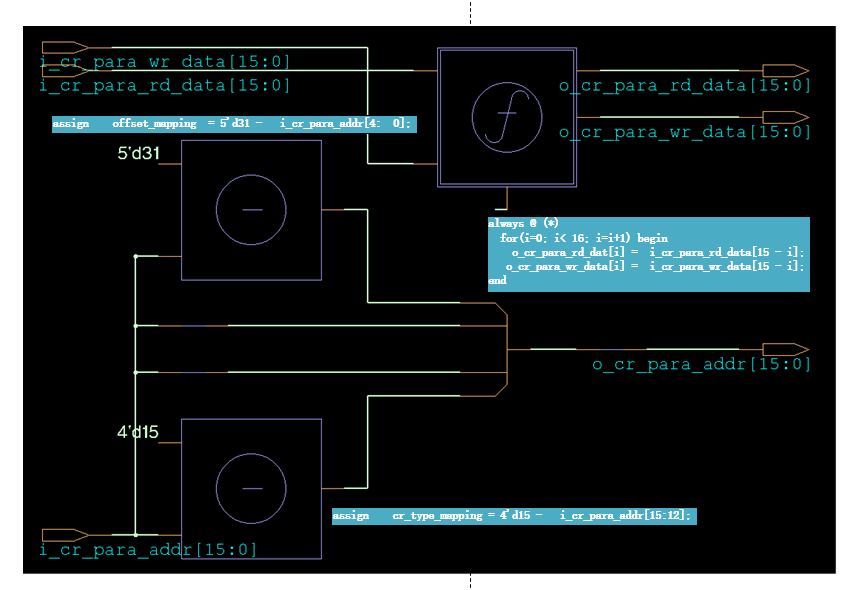
### mem\_reg3

The interface and internal structure are the same as above.

Generate **cmn[63:48]\_b[7:0]** chip select.

### reg\_mapping

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Signal name** | **I/O** | **From** | **To** | **Description/Function** |
| i\_cr\_para\_addr[15:0] | input |  |  | cr\_para\_add before mapping |
| i\_cr para\_rd data[15:0] | input |  |  | cr para\_rd data before mapping |
| i\_cr para wr\_data[15:0] | input |  |  | cr para wr\_data before mapping |
|  |  |  |  |  |
| o\_cr para addr[15:0] | output |  |  | cr\_para\_add after mapping |
| o\_cr para rd data[15:0] | output |  |  | cr para\_rd data after mapping |
| o\_cr para\_wr\_data[15:0] | output |  |  | cr para wr\_data after mapping |



如上图所示，reg\_mapping主要功能是完成对cr\_para\_add/cr\_para\_rd\_data/cr\_para\_wr\_data的映射操作。

## Hardware summarize

cr\_ para\_ addr[15:12]=4'b0101,PHY broadcasts to all PMA lanes.

cr\_para\_ addr[15:12]=4b0110, PHY broadcasts to all RAW PCS lanes.

cr\_para\_ addr[15:12]=4b0111, PHY broadcasts to all RAW PCS AON lanes.

The registers can be operated by firmware/jtag/apb.

Frimware operate register flow:1.Xlane.fsm get order and operate data through cr[7:0]\_mem\_bus ❶ ;2. Xlane.fsm complete register operate with reg\_arbt through cr[7:0]\_reg\_bus❷;2. reg\_arbt complete register operate with registers in every module through cr\_bus❸ ;



# User guide

## 4.1 Configuration Requirements

## 4.3 Registers

# Special Note

# FPGA Verification

# Test Mode Strategy

# Simulation List